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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/007,877	01/10/2006	6483183	25848/81101	9379
31625	7590	09/02/2010	EXAMINER	
BAKER BOTTS L.L.P. PATENT DEPARTMENT 98 SAN JACINTO BLVD., SUITE 1500 AUSTIN, TX 78701-4039			KIELIN, ERIK J	
			ART UNIT	PAPER NUMBER
			3992	
			MAIL DATE	DELIVERY MODE
			09/02/2010	PAPER

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MICROCHIP TECHNOLOGY, INC.

Appeal 2010-000005
Reexamination Control 90/007,877
Technology Center 3900
Patent No. 6,483,183

Before HOWARD B. BLANKENSHIP, SCOTT R. BOALICK, and
KEVIN F. TURNER, *Administrative Patent Judges*.

BOALICK, *Administrative Patent Judge*.

DECISION ON APPEAL¹

¹ The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, or for filing a request for rehearing, as recited in 37 C.F.R. § 41.52, begins to run from the “MAIL DATE” shown on the PTOL-90A cover letter attached to this decision.

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Microchip Technology, Incorporated² appeals under 35 U.S.C. § 134(b) and 35 U.S.C. § 306 from a final rejection of claims 1-18. Claims 19-22 have been cancelled. We have jurisdiction under 35 U.S.C. §§ 134(b) and 306.

We reverse.

STATEMENT OF THE CASE

Reexamination Proceedings

A request for *ex parte* reexamination of U.S. Patent No. 6,483,183 (the ‘183 patent) was filed on January 10, 2006, by Philip W. Woo of Sidley Austin, LLP, Reexamination Control No. 90/007,877.

The ‘183 patent, entitled “Integrated Circuit (IC) Package with a Microcontroller Having an N-bit Bus and up to N-pins coupled to the Microcontroller,” issued November 19, 2002, to Scott Fink, Gregory Bingham, Richard Hull, and Scott Ellison, based on Application No. 09/522,026, filed October 8, 1998. The ‘183 patent is said to be a continuation of Application No. 08/644,916, filed May 24, 1996, now U.S. Patent No. 5,847,450, issued December 8, 1998.

Related Litigation

The ‘183 patent was asserted in two patent infringement suits in *Microchip Tech., Inc. v. Zilog*, No. 2:05-CV-2406 (D. Ariz. filed Aug. 10, 2005) and *Microchip Tech., Inc. v. Luminary Micro, Inc.*, No. 2:06-CV-0986 (D. Ariz. filed Apr. 10, 2006).

² Microchip Technology, Incorporated is said to be the real party in interest and assignee of the patent under reexamination.

Appellant's Invention

Appellant's invention relates to an integrated circuit (IC) package with an IC chip including a microcontroller having an n-bit data bus and up to n pins electrically coupled to the microcontroller. (Abstract.) One or more of the pins are associated with one or more functional blocks to define a specific function for the pin. (Abstract.) The specific function for a pin is selected by an enable signal from a control register coupled to the microcontroller. (Abstract.) The control register selects the appropriate function block upon a command from the microcontroller. (Abstract.)

The Claims

Claims 1 and 5 are exemplary:

1. An integrated circuit (IC) package, comprising:
an IC chip with a microcontroller therein, the microcontroller having an n-bit data bus; and
up to n-pins electrically coupled to the microcontroller.

5. An electronic device comprising:
an integrated circuit package comprising a left side and a right side;
an IC chip with a microcontroller having an n-bit data bus arranged within said integrated circuit package;
a plurality of pins extending from said left side and said right side of said integrated circuit package, said pins being electrically coupled to said microcontroller, wherein the total number of said pins is less than or equal to n.

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*The Rejections*³

Claims 1 and 3 stand rejected under 35 U.S.C. § 103(a) as being obvious over Otake (Japanese Publication No. 3-28985) and Badehi (U.S. Patent 5,455,455), as evidenced by Ling (U.S. Patent Application Publication 2007/0198816 A1) and Appellant's admitted prior art ('183 patent, col. 1, ll. 20-29; col. 3, ll. 30-40) ("APA").

Claims 1-4 stand rejected under 35 U.S.C. § 103(a) as being obvious over Ostler (U.S. Patent 5,787,299).

Claims 1-4 stand rejected under 35 U.S.C. § 103(a) as being obvious over Ostler and Otake.

Claims 5-15 stand rejected under 35 U.S.C. § 103(a) as being obvious over Ostler and Philips Semiconductors Linear Products, *Product Specification NE/SA/SE555/SE555C* 346-352 (Aug. 31, 1994) ("Philips-NE Data Sheet") or, alternatively, over Ostler, Otake and Philips-NE Data Sheet.

Claim 16 stands rejected under 35 U.S.C. § 103(a) as being obvious over Ostler and Hall (U.S. Patent 5,274,778) or, alternatively, over Ostler, Otake and Hall.

Claims 17 and 18 stand rejected under 35 U.S.C. § 103(a) over Ostler, Philips-NE Data Sheet and the APA or, alternatively, over Ostler, Otake, Philips-NE Data Sheet and the APA.

³ The rejection of claims 1-4 under 35 U.S.C. § 102(b) as being anticipated by Daughters (U.S. Patent 4,742,215) as evidenced by the APA and the rejection of claims 1 and 3 under 35 U.S.C. § 102(a) as being anticipated by SGS-Thomson Microelectronics, *CMOS MCU Based Safeguarded Smart Card IC with Modular Arithmetic Processor* (1995) have been withdrawn by the Examiner. (Ans. 2.)

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Appellant relied upon the following in rebuttal to the Examiner's rejection:

JAN AXELSON, THE MICROCONTROLLER IDEA BOOK 1-2 (Lakeview Research 1994) ("The Microcontroller Idea Book").

U. TIETZE & CH. SCHENK, ELECTRIC CIRCUITS DESIGN AND APPLICATIONS 559-561 (Springer-Verlag 1991) ("Tietze/Schenk").

ISSUES

With respect to independent claims 1 and 3, Appellant argues that the combination of Otake and Badehi does not teach or suggest "a microcontroller" because the Examiner improperly interpreted this claim term. (App. Br. 7, 12-14.)

With respect to independent claims 1 and 3, Appellant argues that Ostler does not teach or suggest "the microcontroller having an n-bit data bus; and up to n-pins electrically coupled to the microcontroller." (App. Br. 16, 20-24.) In particular, Appellant argues that Ostler does not teach that the number of external pins is a result-effective variable (App. Br. 20-21) and reducing the number of pins of a microcontroller (App. Br. 21-24). Independent claim 5 recites similar limitations.

Appellant's arguments present the following issues:

1. Has the Examiner erred in finding that the combination of Otake and Badehi teaches or suggests "a microcontroller"?
2. Has the Examiner erred in finding that Ostler teaches or suggests that "the microcontroller having an n-bit data bus; and up to n-pins electrically coupled to the microcontroller"?

FINDINGS OF FACT

The record supports the following findings of fact (FF) by a preponderance of the evidence.

The Microcontroller Idea Book

1. The Microcontroller Idea Book describes a “microcontroller” as a “computer-on-a-chip.” (P. 1, ¶ 2.) “[A] microcontroller is a single-chip computer because it contains memory and I/O [input/output] interfaces in addition to the CPU [central processing unit].” (P.2, ¶ 2.)

Tietze/Schenk

2. Tietze/Schenk describes that one of the functional units for a “microcomputer” includes a microprocessor, also known as a central processing unit (CPU). (P. 559, § 20.1.) The microprocessor or CPU contains three functional blocks: an execution unit, a sequence controller (or sequencer) and a bus interface. (P. 560, § 20.2.1.) The execution unit processes arithmetic and logic instructions (p. 560, § 20.2.1) and includes a data register, an address register and an arithmetic logic unit (ALU) (fig. 20.2). The sequencer includes an instruction decoder and a program counter. (P. 560, § 20.2.1; fig. 20.2.) The bus interface includes a data bus driver, a control bus driver and an address bus driver. (Fig. 20.2.)

*Otake*⁴

3. Otake relates to “a microcomputer suitable for small-scale but multi-variety production and capable of reducing the number of terminals

⁴ Reference is made to the English-language translation provided by Appellant, submitted July 16, 2007.

used for control.” (P. 1, col. 2.) For the microcomputer of its invention a “built-in ROM is not needed.” (P. 2, col. 2.)

4. Figure 1 illustrates a block diagram of an embodiment of the invention of Otake. (P. 2, col. 2.) Figure 1 illustrates an address signal 1, a data signal 2 and a read/write signal 3 transmitted along their respective terminals. Figure 1 also illustrates a program counter 4, shift registers 5 and 6, instruction register 7, instruction decoder 8, and a circuit controller 9.

Ostler

5. Ostler relates to “a microcontroller which includes a pin selection system allowing pins to be used for address/data and special I/O signals.” (Col. 1, ll. 15-18.) In a prior art example, Ostler describes that, for microcontrollers designed to work with a large external memory space, a large number of external pins are required (e.g., 24 pins for 16 megabytes). (Col. 1, ll. 36-39.) Ostler teaches that although external pins can be economized by sharing data and address pins via time division multiplexing, this approach cannot be used for external access by special function devices. (Col. 1, ll. 42-46.) Therefore, Ostler describes a need for “a microcontroller that allows external access pins normally being used for addresses to be used for alternate functions” (col. 1, ll. 51-54), thus “reduc[ing] the number of pins needed for a microcontroller chip having special function circuits” (col. 1, ll. 63-65).

6. A microcontroller system 10 includes a single chip microcontroller 12, external devices 14 and 16, external instruction

memory 18, external data memory 20, a bus interface unit 22, a data bus 24, I/O ports 26-28, an internal peripheral bus 42 (col. 2, ll. 24-39; fig. 1), a special function device 90 (col. 2, ll. 24-39; fig. 1) and a selection circuit 92 (col. 2, ll. 24-39; fig. 1).

7. The microcontroller 12 communicates with the external instruction memory 18 and the external data memory 20 through the bus interface unit 22 and the data bus 24 having a 24 bit capability. (Col. 2, ll. 32-35.) The microcontroller 12 communicates with the external devices 14 and 16 through I/O ports 26-28. (Col. 2, ll. 36-38.) Figure 2 illustrates that the data bus 24 is accessible by pins 111. External access of the special function devices 90 to the microcontroller 12 is also provided through the data bus 24 by the selection circuit 92. (Col. 3, ll. 3-5; fig. 3.) In one example, Figure 3 illustrates a system in which eight bits of a 24 bit external bus can be selected for an alternative function. (Col. 3, ll. 55-60; fig. 3.)

Ling

8. Ling relates to “an emulation system for a single-chip multi-microcontroller.” (¶ [0002].) “A microcontroller (microcontroller unit, MCU), which has all the functions of a complete computer, is almost equal to a miniature computer and can work independently without any auxiliary circuit; therefore, a microcontroller is also referred to as a single-chip microcomputer.” (¶ [0004].)

Badehi

9. Badehi “relates to methods and apparatus for producing integrated circuit devices.” (Col. 1, ll. 9-10.) In the “Background of the

Invention” section, Badehi describes that “[a]n essential step in the manufacture of all integrated circuit devices is known as ‘packaging’ and involves mechanical and environmental protection of a silicon chip which is at the heart of the integrated circuit as well as electrical interconnection between predetermined locations on the silicon chip and external electrical terminals.” (Col. 1, ll. 14-19.)

Philips-NE Data Sheet

10. A “Pin Configurations” figure from the Philips-NE Data Sheet illustrates a top view of two integrated circuit packages (“D, N, FE Packages” and “F Package”) with pins extending from a left side of both packages and pins extending from a right side of both packages. (P. 346.)

Hall

11. In the “Background of the Invention” section, Hall describes that “programmable read only memories (EPROMs) and electrically erasable programmable read only memories (EEPROMs) have been employed in a wide variety of circuits, including, for example, stand alone memory chips and memory locations within microprocessors and microcontrollers.” (Col. 1, ll. 15-21.)

ANALYSIS

Claims 1-4

With respect to the first issue, we are convinced by Appellant's argument (App. Br. 7, 12-14) that the combination of Otake and Badehi does not teach or suggest "a microcontroller," as recited in claims 1 and 3.

The Examiner found that the claimed "microcontroller" corresponds to the "microcomputer" of Otake. (Ans. A-3.) The Examiner cited Badehi as evidence that a "microcontroller" is equivalent to a "microcomputer." (Ans. 8, A-4.) We do not agree.

Otake teaches a "microcomputer" with a reduced number of terminals that does not include a read-only memory (ROM). (FF 3.) However, as evidenced by the Microcontroller Idea Book, a "microcontroller" is defined as a "computer-on-a-chip" that includes a central processing unit (CPU), a memory and input/output interfaces. (FF 1.) Thus, the "microcomputer" of Otake is not a "microcontroller" because it does not include a memory. (See FF 1.)

Furthermore, Figure 1 of Otake illustrates a block diagram of the microcomputer, including an address signal 1, a data signal 2, a read/write signal 3, a program counter 4, shift registers 5 and 6, instruction register 7, instruction decoder 8, and a circuit controller 9. (FF 4.) However, as evidenced by Tietze/Schenk, a "CPU" includes an execution unit, a sequence controller and a bus interface. (FF 2.) Figure 20.2 of Tietze/Schenk illustrates that the "execution unit" includes a data register, an address register and an arithmetic logic; the "sequencer" includes an instruction decoder and a program counter; and the "bus interface" includes

a data bus driver, a control bus driver and an address bus driver. (FF 2.) Thus, in comparing Figure 1 of Otake with Figure 20.2 of Tietze/Schenk, the “microcomputer” of Otake is a “CPU” rather than a “microcontroller.” (See FF 2, 4.) Badehi, which was relied upon by the Examiner for its teaching of integrated circuit packaging (Ans. A-4; FF 9), does not cure the above-noted deficiencies of Otake.

The Examiner argues that Ling provides evidence to support the position that a “microcontroller” is equivalent to a “microcomputer.” (Ans. 8.) However, Ling teaches that a “microcontroller . . . has all the functions of a complete computer.” (FF 8.) As discussed previously, the “microcomputer” of Otake is a CPU and does not have all the functions of a complete computer.

Therefore, the Examiner has erred in finding the combination of Otake and Badehi teaches or suggests “a microcontroller,” as recited in claims 1 and 3.

We conclude that the Examiner has erred in rejecting independent claims 1 and 3 under 35 U.S.C. § 103(a) as being obvious over Otake and Badehi.

With respect to the second issue, we are convinced by Appellant’s argument (App. Br. 16, 20-24) that Ostler does not teach or suggest “the microcontroller having an n-bit data bus; and up to n-pins electrically coupled to the microcontroller” as recited in independent claims 1 and 3.

The Examiner acknowledged that Ostler does not teach or suggest “the microcontroller having an n-bit data bus; and up to n-pins electrically coupled to the microcontroller.” (See Ans. A-5.) However, the Examiner

concluded that this claim feature would have been obvious because “claiming the specific reduction in pins to be up to the number of pins in the data bus is merely a result effective variable that follows from optimizing the reduction of the number of pins at the explicit suggestion in *Ostler* to reduce the number of pins.” (Ans. A-5.) We do not agree.

Ostler teaches a microcontroller with a pin selection system that allows the pins to be used for address/data signals and special I/O signals from special function circuits. (FF 5.) *Ostler* also teaches a microcontroller 12 that communicates with an external instruction memory 18 and an external data memory 20 through a data bus 24, accessible by pins 111. (FF 6-7.) *Ostler* further teaches external access to special function devices 90 through the data bus 24 and pins 111. (FF 7.) In other words, *Ostler* teaches that instead of increasing the number of external pins to accommodate the special function circuits, each of the existing external pins has the additional capability of transmitting address/data signals and special I/O signals from special function circuits. (See FF 6-7.) Thus, *Ostler* does not teach or suggest reducing the total number of external pins, but instead maintains the existing number of external pins. (See FF 5.)

Furthermore, *Ostler* does not provide any recognition that the number of pins 111 is a result-effective variable (i.e., varying the number of pins 111 achieves a recognized result). Therefore, the number of pins 111 in *Ostler* has not been shown to be a parameter subject to optimization. See *In re Antonie*, 559 F.2d 618, 620 (CCPA 1977).

Therefore, the Examiner has erred in finding that Ostler teaches or suggests “the microcontroller having an n-bit data bus; and up to n-pins electrically coupled to the microcontroller,” as recited in claims 1 and 3.

In the alternative, the Examiner relied upon Otake, for its teaching of “the microcontroller having an n-bit data bus; and up to n-pins electrically coupled to the microcontroller.” (Ans. A-7.) However, Otake does not cure the above-noted deficiencies of Ostler because, as discussed previously, Otake does not teach or suggest a “microcontroller,” but instead relates to a microcomputer in which a “built-in ROM is not needed” (FF 3).

We conclude that the Examiner erred in rejecting independent claims 1 and 3 under 35 U.S.C. § 103(a) as being obvious over Ostler or over Ostler and Otake. Claims 2 and 4 depend from independent claims 1 and 3, and we likewise conclude that the Examiner erred in rejecting these claims under 35 U.S.C. § 103(a) as being obvious over Ostler or over Ostler and Otake for the reasons discussed with respect to independent claims 1 and 3.

Claims 5-15

Independent claim 5 recites limitations similar to those discussed with respect to independent claims 1 and 3. We conclude that the Examiner erred in rejecting this claim, as well as claims 6-15, which depend from claim 5, for the reasons discussed with respect to independent claims 1 and 3. The Philips-NE Data Sheet, which was relied upon by the Examiner for its teaching of “an integrated circuit package comprising a left side and a right side” and “a plurality of pins extending from said left side and said right side of said integrated circuit package” (Ans. A-8; FF 10), does not cure the

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above-noted deficiencies of Ostler. Otake also does not cure the above-noted deficiencies of Ostler for the reasons previously discussed.

Claim 16

Claim 16 indirectly depends from independent claim 5 and the Examiner has erred in rejecting this claim for the reasons discussed previously with respect to independent claim 5. Hall, which was relied upon by the Examiner for its teaching of “wherein said memory device is a SRAM, DRAM, EPROM, EEPROM, ROM, PROM or a logic device” (Ans. A-13 to -14; FF 11), does not cure the above-noted deficiencies of Ostler. Otake also does not cure the above-noted deficiencies of Ostler for the reasons previously discussed.

Claims 17 and 18

Claims 17 and 18 indirectly depend from independent claim 5 and the Examiner has erred in rejecting these claims for the reasons discussed previously with respect to independent claim 5. The APA, which was relied upon by the Examiner for its teaching of “a bi-directional I/O port unit” and “a serial programming unit” (Ans. A-14 to -15), does not cure the above-noted deficiencies of Ostler. Otake also does not cure the above-noted deficiencies of Ostler for the reasons previously discussed.

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CONCLUSION

Based on the findings of fact and analysis above, we conclude that the Examiner has erred in rejecting claims 1-18.

DECISION

The rejection of claims 1-18 is reversed.

REVERSED

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