



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
95/001,166	04/03/2009	7287109	2805.003REX8	7774
22852	7590	09/01/2011	EXAMINER	
FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP 901 NEW YORK AVENUE, NW WASHINGTON, DC 20001-4413			ESCALANTE, OVIDIO	
			ART UNIT	PAPER NUMBER
			3992	
			MAIL DATE	DELIVERY MODE
			09/01/2011	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

---

BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

---

*Inter Partes*  
RAMBUS, INC.  
Patent Owner

v.

NVIDIA CORP.

\_\_\_\_ Requestor \_\_\_\_

Appeal 2011-005255  
Reexamination Control No. 95/001,166  
United States Patent 7,287,109  
Technology Center 3900

---

Before ALLEN R. MacDONALD, KARL D. EASTHOM, and  
STEPHEN C. SIU, *Administrative Patent Judges*.

EASTHOM, *Administrative Patent Judge*.

DECISION ON APPEAL

Appeal 2011-005255  
Reexamination Control 95/001,166  
Patent 7,287,109

Appellant, patent owner Rambus, appeals under 35 U.S.C. §§ 134(b) and 306 from the Examiner's Right of Appeal Notice (RAN) rejecting claims 1-25 of U.S. patent 7,287,109 B2 to Barth et al., *Method of Controlling a Memory Device Having a Memory Core* (Oct. 23, 2007). Respondent, third party requestor NIVIDIA, cross-appeals from the RAN for failure to adopt some of the proposed rejections (Cross App. Br. 3-6) and supports the Examiner's decision to adopt Respondent's proposed anticipation and double patenting rejections based on one of Rambus's prior art patents (*see* Req. Resp. Br. 4). No pending claims have been confirmed. We have jurisdiction under 35 U.S.C. §§ 134(b) and 315.

We AFFIRM the anticipation rejection of claims 1-25, reverse the double patenting rejection, and decline to reach the non-adopted rejections.

#### STATEMENT OF THE CASE

Appellant and Requestor refer to several related judicial and other proceedings including *inter partes* and *ex parte* reexaminations, International Trade Commission proceedings, and Federal District Court and Circuit Court proceedings in their briefs. An oral hearing of this appeal transpired on May 4, 2011 and was subsequently transcribed.

#### *The '109 Patent (Factual Findings)*

D1. The '109 patent discloses at least two embodiments for operating a DRAM (dynamic random access array) memory device. (Col. 1, ll. 20-23; col. 9, l. 26 to col. 10, l. 67.) The disclosed DRAM comprises control logic, a clock, a receiver, transmitter, DRAM memory core arrays, and caches. (*See* Fig. 6.) The first embodiment employs a strobe signal, the second does not. In both embodiments, a memory device (e.g., a DRAM) receives

command control information causing it to begin a process for reading data from, or writing data to, the memory core. (Col. 9, l. 26 to col. 10, l. 67.)

D2. In the first embodiment, the strobe embodiment, if the command control information specifies: 1) a write mode, the strobe signal subsequently causes the memory device to accept data from a data bus (i.e., for writing the data into the memory device); or, 2) a read mode, the strobe signal subsequently causes the memory device to transfer data to the bus (i.e., after reading data from the memory device core). (*See* col. 7, ll. 36-57; Fig. 8.) The strobe signal causes the transfer to occur several clock cycles after the strobe signal. (*See* col. 9, ll. 41-51 (discussing latency); Fig. 12 (operations 0 and 3 showing clock cycle lags between the strobe and data).)

One benefit of the '109 patent system stems from latency minimization, resulting in a relatively free data bus for other data transfers – i.e., the command control information tells the memory device to prefetch the desired data from the memory core and the device then waits for the strobe signal to send the data: “Because the initial data packet to be transmitted by the DRAM has been prefetched from the core, the data packet can be transmitted over the channel with minimal delay from when the strobe signal ultimately arrives.” (Col. 9, ll. 37-40.)

In addition to the strobe signal, the first embodiment employs a terminate signal to indicate when to stop sending the data. The '109 patent describes aspects of the first embodiment in terms of prior art systems as follows:

According to one aspect of the invention, the command control information within a request packet no longer contains size information. Rather the DRAM is configured to start and end the transmission of data based on data transfer control

information sent by the controller to the DRAM separate from and subsequent to the transmission of the command control information. According to one embodiment, the data transfer control information includes data transfer start information (a 'strobe signal') sent from the controller to indicate when the DRAM is to begin sending data, and a data transfer end information (a 'terminate signal') to indicate when the DRAM is to stop sending data. The number of clock signals that elapse between the transmission of the strobe signal and the terminate signal indicates the size of the data transfer.

(Col. 8, l. 63 to col. 9, l.10.)

As mentioned above, the data transfer control information which controls the timing of the data transfer associated with a request packet is sent separately from the command control information to which it corresponds. According to another aspect of the invention, the timing of the data transfer control information is variable relative to the timing of the corresponding request packet. That is, the number of clock cycles between the transmission of a request packet and the transmission of the strobe signal to begin the transfer specified in the request packet may vary from transaction to transaction.

(Col. 10, ll. 41-51.)

D3. In a second "alternate" embodiment, described under a section heading titled "Decoupled Data Transfer Control Information" (109 patent, col. 10, l.25), a controller varies the timing of data transmission without use of the above-described strobe signal:

According to an alternate embodiment of the invention, the amount of time that elapses between the transmission of a request packet and the transmission of the data specified in a request packet is varied without the use of strobe and terminate signals.

In this embodiment, the reset [sic: request] packet contains a delay value that indicates to the DRAM when the data specified in the request packet will begin to be sent relative

to the time at which the request packet is sent. The DRAM would include a counter to count the clock cycles that elapse from the arrival of the request packet in order to send or receive the data specified in the request on the appropriate clock cycle. Because the controller may vary the latency between the request packet and the data transmission, the controller is able to dynamically adjust the operative interleave on the channel . . . .  
(Col. 10, ll. 52-67.)

D4. According to the '109 patent, in contrast to the two embodiments discussed *supra*, prior art systems control the data transfer timing based on a fixed number of clock cycles after the clock cycle on which a request packet arrives. As such, these “prior art systems [are] inflexible with respect to how control and data signals may be interleaved” (col. 10, ll. 37-39) because the timing delay value in such prior art systems is fixed in a register within a DRAM. (*See* col. 10, ll. 28-67.)

#### *Exemplary Claims*

Exemplary claims 1 and 7 of the '109 patent under reexamination follow:

1. A method of controlling a memory device having a memory core, wherein the method comprises:

providing control information to the memory device, wherein the control information includes a first code which specifies that a write operation be initiated in the memory device;

*providing a signal to the memory device, wherein the signal indicates when the memory device is to begin sampling write data, wherein the write data is stored in the memory core during the write operation;*

providing a first bit of the write data to the memory device during an even phase of a clock signal; and

providing a second bit of the write data to the memory device during an odd phase of the clock signal.

7. The method of claim 1, further comprising providing, to the memory device, a signal that indicates when the memory device is to terminate the sampling of the write data.

### *Rejections*

The Examiner adopted a proposed rejection of claims 1-25 under 35 U.S.C. 102(e) as anticipated based on a Rambus patent to Farmwald et al., *A Memory Device Which Samples Data After an Amount of Time Transfers,*” Corp.) (1982) [hereinafter Farmwald].

The Examiner also rejected claims 1-6, 11-13, and 20-24 based on nonstatutory obviousness-type double patenting over claims 1-3, 8, and 9 of Farmwald.<sup>1</sup>

### ISSUES

Appellant’s and Respondent’s Briefs raise the following issues:

Does Farmwald disclose a signal as recited in claim 1?

Does Farmwald disclose a signal that indicates when the memory device is to terminate the sampling of the write data as recited in claim 7?

Did the Examiner show that some of Farmwald’s claims render certain of the ‘109 patent’s claims unpatentable based on double patenting?

### ADDITIONAL FINDINGS OF FACT

#### *Farmwald*

F1. Farmwald discloses using request packets which can vary the data block transfer time in manner which is similar to the alternate (delay

---

<sup>1</sup> The Examiner states that this rejection is a modified version and partial adoption of Requestor’s proposal. (See RAN 40.)

value/non-strobe) embodiment of the '109 patent (D3), to determine when to read or write data from a memory device:

The data block transfer occurs later at a time specified in the request packet control information, preferably beginning on an even cycle. A device begins a data block transfer almost immediately with a device-internal phase as the device initiates certain functions, such as setting up memory addressing, before the bus access phase begins. The time after which a data block is driven onto the bus lines is selected from values stored in slave access-time registers. The timing of data for reads and writes is preferably the same; the only difference is which device drives the bus.

(Col. 9, ll. 18-30.)

F2. A request packet 22 contains address data and typically 1.5 bytes of control data, with control 1) operations such as write or read and 2) the timing of the data transfer, the latter of which is specified, indirectly, or directly, in different bits of the control bytes. (Fig. 4, col. 9, ll. 31-53.)

F3. More specifically, the data transfer timing information arrives in the request packet in the form of an "op code," and this particular op code can either be used to select a certain register in the slave DRAM memory device which stores the (delay value) timing information, or the op code can indirectly indicate pre-selected (delay value) access times. (Col. 9, l. 46 to col. 10, l. 5.)

F4. With further respect to this delay value, Farmwald dependent claim 28 recites "outputting a value to the memory device, wherein the value is representative of the delay time; and outputting a second operation to the memory device, wherein the second operation code instructs the memory device to internally store the value."

Appeal 2011-005255  
Reexamination Control 95/001,166  
Patent 7,287,109

F5. Farmwald refers to the invention as comprising “11 signals,” including two bus data signals, clock signals, power, ground and address valid signals, and Farmwald states that such “[s]ignals are driven onto the bus.” (Col. 8, ll. 24-37.)

#### PRINCIPLES OF LAW

Claims “must be read in view of the specification. . . . [T]he specification ‘is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.’” *Phillips v. AWH Corp.*, 415 F.3d, 1303, 1315 (Fed. Cir. 2005) (en banc) (quoting ?). Also, “the ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application.” (*Id.* at 1313) (internal citations omitted).

“Even when the specification describes only a single embodiment, the claims of the patent will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using ‘words of manifest exclusion or restriction’.” *Leibel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004) (citation omitted). “Indeed, a claim interpretation that would exclude the inventor’s device is rarely the correct interpretation; such an interpretation requires highly persuasive evidentiary support . . . .” *Modine Mfg. Co. v. U.S. Intern. Trade Comm’n*, 75 F.3d 1545, 1550 (Fed. Cir. 1996) (cited with approval by *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1583) (Fed. Cir. 1996)).

## ANALYSIS

Appellant maintains that Farmwald does not anticipate independent claims 1, 12, and 20, primarily because the Examiner's interpretation of "providing a signal" is too broad. (App. Br. 7, 20 (stating that claims 12 and 20 rise and fall with claim 1).) Appellant maintains that the '109 patent provides "[e]xamples of 'signals' . . . [which] include 'strobe signals' and terminate signals.'" (App. Br. 21-22.) Appellant relies on Rambus's expert, Mr. Murphy, and maintains that, in the '109 patent, the command and control information is separate from, and decoupled from, the signal which indicates when the memory device is to begin writing. (App. Br. 10 (citing Murphy Decl. at ¶¶ 14-20, 39-47).) Appellant also argues that claim 1 recites two separate steps, 1) providing control information, and 2) providing a signal to the memory device, with the latter step following the former. (App. Br. 9-10, 21-22 (citing Murphy Decl. at ¶¶ 40-44).)

Appellant frames the central anticipation issue on appeal as "whether the storing of a value in an access-time register as described in the '037 patent anticipates or renders patentably indistinct the 'providing a signal' step in the '109 patent." (App. Br. 12.)

Claim 1 does not recite a "strobe signal," but instead more generally recites a "signal." As such, the Examiner reasons that the claimed "signal" need not be a strobe signal. (RAN 9.) Respondent, in agreement with the Examiner, points out that the '109 patent neither provides a definition for "signal," nor a disclaimer for precluding other signals according to the plain meaning of "signal." (Req. Resp. Br. 6-7.) As to the plain meaning, Respondent points to an IEEE Standard Dictionary for a signal as "the physical representation of data.'" (Resp. Br. 8) (maintaining at n.5 that

Appeal 2011-005255  
Reexamination Control 95/001,166  
Patent 7,287,109

Rambus and Rambus's expert cite the same IEEE definition in other Rambus litigation.) The Examiner also points out that the '109 patent generally describes signal lines as carrying all manner of data, including clock signals and other transmissions to the memory devices. (Ans. 11; *accord* F5 (Farmwald broadly describing various signals).)

For the reasons that follow, Appellant's arguments fail to demonstrate that claim 1 requires a strobe signal so as to preclude other plain meanings for signal, and particularly, the signals involved in the non-strobe embodiment in the '109 patent (*see* D3, D4) and the similar system in Farmwald (*see* F1-F5).

Appellant describes the Farmwald delay value system, *inter alia*, as follows: "The amount of time that must transpire may be determined by a value stored in a register within the memory device." (App. Br. 10-11 (citation omitted).) Appellant also describes this system as including a request packet that has different bits, in particular:

The first bit, AccessType[0], is a read/write switch that indicates whether the requested operation is a read or write. . . . AccessType [1:2] bits specify what access-time register, Access RegN, the device should use. As noted, an access-time register is a register within the memory device that holds an access time value representative of the time a device must wait from receiving a transaction before responding to it. After the specified time has passed, the memory device responds to the request.  
(App. Br. 11.)

The Examiner relies on similarities between Farmwald's programmable delay value (*see* F1-F4) and the '109 patent's non-strobe delay value embodiment (D3) to show anticipation:

the disclosed [109' patent's] "delay value" is characterized as a signal since it [sic] [is] provided to the memory device for signaling the memory device to perform a specific function. In this case the delay value signal indicates that the memory device should wait a certain amount of clock cycles before outputting data. This signal is the same as disclosed by . . . Farmwald. That is, the number of clock cycles to wait before data is sampled is received from a controller as a value.  
(RAN 10.)

The arguments and findings of record show that there are no material factual disputes about the delay value systems in Farmwald or the '109 patent – i.e., the disputes turn on claim interpretation. That is, Farmwald, in a manner similar to the '109 patent, discloses a controller which provides separate instructions/codes in a request packet – (at least) 1) one for designating a read or write operation, and 2) another for designating a delay value. (*Compare F1-F5 with D3-D4.*)

Appellant's arguments notwithstanding, Farmwald's two separate instructions/codes satisfy the disputed first two claim steps in claim 1: the write or read bit constitutes providing control information, while transmitting, storing or retrieving the delay value constitutes providing a signal to the memory device. For example, Farmwald's time delay value information is first provided by the controller, inserted into a request packet, and then, separately from the providing control information step associated with the read/write code, stored in, and thereafter retrieved from, an access-time register. Still further, Farmwald's system implicitly compares a clock signal counter to this register-stored delay value, and thereafter implicitly generates another signal for completing the data read or write operation upon a determination that the clock counter equals the delay value, thereby

implying at least two more separate steps (i.e., comparing and signaling).<sup>2</sup>  
(*See* F1-F4; *accord* App. Br. 11-12 (describing Farmwald’s memory device as waiting “passively” for the specified number of clock signals and specified delay value to expire). )

Claim 1 recites that “the control information includes a first code” which means, in addition to the first code (i.e., Farmwald’s read/write bit), that the control information may or may not include other information such as the recited signal: i.e., Farmwald’s delay value, which is either: 1) in the request packet; 2) stored in an access-register; 3) provided for comparison to a clock; and/or 4) implicitly used to generate another implicit signal after the comparison to signify a match. In support of the claim construction under which the recited control information does not preclude the recited signal (i.e., with both in the same request packet of Farmwald), Respondent correctly notes (Req. Resp. Br. 9-10) that the ‘109 patent describes “control information” as including the strobe signal (D2) and the delay value (*see* D3 (non-strobe embodiment described under the heading, “Decoupled Data Transfer Control Information”); App. Br. 22 (arguing that the delay time “falls into the ‘providing control information’ bucket ).) Hence, the strobe signal and the delay value constitute similar “control information” and perform similar functions, reasonably indicating, like the plain meaning of

---

<sup>2</sup> In addition, pre-programming the access-time registers with time delay values (which correspond to the delay op code in a request packet) implicitly involve separate steps – i.e., apart from steps involved in the request packet which has the read/write bit and the delay value op code. (*See* F3, F4.) Appellant refers to Farmwald’s storing of values in the access-time register using a control access register (App. Br. 12) and to Farmwald’s “process of pre-programming an access-time register on a DRAM” (App. Br. 21).

Appeal 2011-005255  
Reexamination Control 95/001,166  
Patent 7,287,109

the term “signal” (*see* IEEE Dictionary definition cited *supra*; F5 (designating a wide array of signals)), that both constitute a “signal.”

Appellant’s related arguments, embracing testimony by expert Mr. Murphy, that the ‘109 patent separates the “command and control information” from the strobe and terminate signals, are not commensurate in scope with claim 1 which neither recites “*command* control information” nor any separation. (*See* App. Br. 10 (citing Murphy Decl.)) Moreover, these arguments relate to the first embodiment in the ‘109 patent, the strobe signal embodiment. For example, according to the ‘109 patent, “command control information” includes information within a request packet, while “transfer control information” includes the strobe signal. (D2.) Claim 1 recites the generic phrase “control information includes a first code;” and therefore, claim 1 does not preclude other control information, such as a delay value signal, as part of the “control information” in a request packet.

Based on the ‘109 patent and the generic claim language, skilled artisans reasonably would have considered “providing a signal” as transmitting or otherwise providing additional control information (i.e., additional to a first code) within a request packet, such as the variable delay value signal. Alternatively, skilled artisans would have considered either 1) storing the delay value in the access-register, 2) retrieving it, or 3) comparing it to a clock value and generating another (implicit) signal, as Farmwald provides, as also constituting “providing a signal,” as recited in claim 1. Under any of these latter alternatives, Farmwald’s delay value

signal, as provided at these latter stages in the memory device, is provided separately from the “control information” provided in the request packet.<sup>3</sup>

As Respondent further points out, even the strobe signal embodiment does not cause an immediate write or read operation, because there is some delay thereafter before any action occurs. (Req. Resp. Br. 10-11; *accord* D2.) This fact is not in dispute. As such, Appellant’s argument that sending Farmwald’s delay value does not constitute providing a signal, because it does not indicate “when the memory device is to begin sampling write data,” as claim 1 requires (App. Br. 22-23), lacks merit. Claim 1 does not preclude the signal, in this case the delay value as either specified in Farmwald’s control packet or as later retrieved from a register and compared to a clock signal, to indicate a future time “when” to begin writing or sending data into or from the DRAM. (And under the latter “compared to a clock” alternative, “when” would be immediate.)

In further attempting to show that Farmwald does not anticipate claim 1, Appellant states that “the ‘037 patent [i.e., Farmwald] discloses a type of prior art system that the ‘109 patent describes as ‘inflexible’.” (App. Br. 11, *accord* App. Br. 23.) This argument improperly characterizes the Farmwald system and fails to recognize that it is similar to the ‘109 patent’s delay value embodiment. (*Compare* F1-F4 *with* D3.)

According to the ‘109 patent, the prior art “inflexible” systems provide a fixed (stored) latency and preclude data and control interleaving on the data bus. In contrast, the delay value (non-strobe) embodiment allows the controller to “vary the latency between the request packet and the

---

<sup>3</sup> Claim 1 does not preclude providing the signal from one part of the memory device to another part of it.

data transmission, [and] the controller is able to dynamically adjust the operative interleave on the channel.” (D3.) This delay value embodiment is described in a section titled “Decoupled Data Transfer Control Information,” implying one reason (i.e., decoupling) for its flexibility. (D3.) Hence, the ‘109 delay value embodiment is not “inflexible.”

And similar to the ‘109 patent’s delay value embodiment, Farmwald’s delay value system provides similar flexibility; i.e., more than the inflexible prior art systems - by allowing the delay value to be varied by the controller, for example, by sending a request packet having a code for selecting different access-time registers each storing a different delay value, by otherwise programming and storing different values in such access-time registers, or by sending different operation codes representing different delay values. (*See* F1-F4 and Appellant’s arguments describing Farmwald as discussed *supra*.)

Appellant also argues in their Rebuttal Brief that Rambus showed that the non-strobe embodiment “was an unclaimed embodiment.” (App. Reb. Br. 7.) To the contrary, Appellant’s arguments at most show that “the *specification* unambiguously distinguishes that embodiment” (App. Reb. Br. 7 (quoting App. Br. 20) (emphasis added by the Board).) These arguments fail to demonstrate that claim 1 fails to encompass both the strobe and the non-strobe embodiment. (*See* App. Br. 19-20; App. Reb. Br. 7-9.) Moreover, Appellant cites to the ‘109 patent Specification to show support for the claim terms, but issues qualifiers to preclude an overly narrow claim interpretations based thereon: “The citations do not . . . recite every instance where the claim term is described . . . . As such, Rambus does not intend the

Appeal 2011-005255  
Reexamination Control 95/001,166  
Patent 7,287,109

present citations to impliedly result in any admission or inappropriate disclaimer of patent scope.” (App. Br. 5.)

This is not a situation in which the ‘109 patent discloses only a single embodiment. Rather, Appellant’s claim construction would exclude one of the two disclosed main embodiments. “[A] claim interpretation that would exclude the inventor’s device is rarely the correct interpretation . . . .” *Modine Mfg. Co.* 75 F.3d at 1550. Further, in a related patent, the ‘405 patent, Rambus claims a strobe signal, indicating here that the strobe signal embodiment is not the only embodiment embraced. *See Liebel-Flarsheim*, 358 F.3d at 910 (juxtaposition of claims with express limitation and without express limitation indicates the latter claims do not contain the limitation).<sup>4</sup>

Also, when a patent refers to “an alternate embodiment of *the invention*,” as the ‘109 patent does (D3 (emphasis added)), it implies that a broad claim encompasses the embodiment. *See Edwards Life Sciences LLC v. Cook Inc.*, 582 F.3d 1322, 1330 (2009) (characterizing *SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys. Inc.* 242 F.3d 1337, 1343 as “construing term to include feature characterized as ‘the present invention’”); *cf. Edwards*, 582 F.3d at 1330 (citing additional similar precedent and holding that the consistent interchanging of “interluminal graft 10” with “graft 10,” use of the phrase, “as defined above,” and frequently describing an “interluminal graft” as “‘the present invention’” or “‘this invention’” created a narrowing definition of graft to mean an interluminal graft). Disclosing another embodiment as “the invention” cuts

---

<sup>4</sup> Relying on the doctrine of claim differentiation and comparing dependent and independent claims albeit within the same patent.

Appeal 2011-005255  
Reexamination Control 95/001,166  
Patent 7,287,109

against any type of *Edwards*-based limiting inference, and elicits an intention to embrace both of the embodiments described.

Based on the foregoing discussion, Rambus did not clearly limit the signal to a strobe signal. Under analogous circumstances involving another Rambus patent, our reviewing court held that the ordinary term “bus” could not be read restrictively as a “multiplexed bus” even though the patentee described the “present invention” in terms of a “multiplexed bus” in isolated portions of the specification because “the remainder of the specification and the prosecution history shows that Rambus did not *clearly* disclaim or disavow such claim scope in this case.” *Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1094-95 (Fed. Cir. 2003); *accord Leibel-Flarsheim*, 358 F.3d at 906 (“[T]he claims of the patent will not be read restrictively unless the patentee has demonstrated a *clear intention* to limit the claim scope using ‘words of manifest exclusion or restriction’.” (Citation omitted, emphasis added)). Appellant here not only fails to present persuasive evidence showing a clear intention in the ‘109 patent Specification which would support a limiting interpretation, but Appellant intentionally obfuscates by arguing that the claims are not limited to specific descriptions cited to in the Brief, as noted above. (*See App. Br. 5.*)

Claim 7, which depends from claim 1 and which Appellant groups together with claims 8, 9, 14-16, and 25 (App. Br. 20), requires “a signal that indicates when the memory device is to terminate the sampling of the write data.” Claim 14 recites a similar limitation and claim 25 similarly recites “a signal that indicates when the memory device is to end the transfer operation.”

To satisfy this signal (which indicates the end or termination of data writing or transferring) limitation, the Examiner and Requestor rely on Farmwald's disclosure of a data block value in a "BlockSize field" within a request packet. (*See* App. Br. 20 (discussing the respective positions).) This block value is variable, and ultimately, tells the system when to end transmission or writing of data based on the data block size. (*See* Req. Resp. Br.11-12; '037 patent, col. 11, l. 46 to col. 12, l. 2.)

But Appellant asserts a claim distinction over this block size value because it is "exactly the 'size information' that the '109 patent explained is eliminated by implementing the disclosed terminate signal." (App. Br. 24 (relying on Murphy Decl. at ¶¶45-47).) Respondent maintains that this disclosed distinction "is merely recognition of the problem that the Patent Owner has created for itself by choosing overly broad claim language." (Req. Resp. Br. 12.)

As Appellant indicates, the '109 patent does state that "according to one aspect of the present invention, the command control information within a request packet no longer contains size information." (App. Br. 24, citing the 109' patent at col. 8, ll. 63-65.) This statement, distinguishing a packet size value system for terminating data transmission in the prior art, by itself, weighs in Appellant's favor for limiting the recited signal in claims 7, 14, and 25. On the other hand, other factors weigh against Appellant's position.

First, the '109 patent also states that "transmitting a terminate control signal to the DRAM" is part of "one prior art request-oriented system." (109' patent, col. 8, ll. 51-53.) In other words, the '109 patent admits that "terminate control signal[s]" were used in prior art systems. Thus, since the '109 patent admits that both "terminate control signal" systems and block

Appeal 2011-005255  
Reexamination Control 95/001,166  
Patent 7,287,109

size terminating information systems were known, it follows that claim 7, which broadly recites “a signal that indicates when . . . to terminate . . . sampling” and depends from claim 1, does not necessarily rely on, preclude, or distinguish over, either one of these two prior art methods of ending data transmission.<sup>5</sup>

Next, the ‘109 patent describes “data transfer end information (a ‘terminate signal’) to indicate when the DRAM is to stop sending data,” and specifies that, according to an aspect of the invention, such a “terminate signal” is transmitted without block size information and separately from other command control information in a request packet. (*See* ‘109 patent, col. 8, l. 63 to col. 9, l. 10.) In contrast to this disclosure, independent claims 7, 14 and 25 do not specifically 1) recite this disclosed “‘terminate signal’,” 2) preclude block size information, and 3) require the signal for indicating an end of transmission to be transmitted separately from block size information. As such, claims 7, 14, and 25 are broader than any disclosed or preferred embodiment and do not distinguish over the ‘037 patent’s variable block size information employed for ceasing data reads or writes. In addition, Appellant’s failure to recite a quoted term “‘terminate signal’” from the ‘109 patent Specification, the recitation of the

---

<sup>5</sup> While the dual admissions indicate that claim 7 logically does not rely solely on either known system as a patentable distinction, in addition, an applicant typically cannot rely on an admitted prior art element to distinguish a claim. *See Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 1570 (Fed. Circ. 1988)(“A statement in a patent that something is in the prior art is binding on an applicant and patentee for determinations of anticipation and obviousness.”)(citing *In re Nomiya*, 509 F.2d 566, 571 n.5 (CCPA 1975) (admission that certain matter is prior art means it is prior art for all purposes)).

term “end” instead of “terminate” in claim 25 which is grouped with claim 7, and other statements made disavowing a limiting effect based on the Specification (App. Br. 5), manifest at most, a *vague* intention to inferentially limit the claims, as opposed to a *clear* intention as *Leibel-Flarsheim* requires. As such, the claimed “signal” is not limited to the ““terminate signal”” embodiment.

Finally, the ‘109 patent interchanges the terms “signal” and “information” when discussing the similar functional operations of ending (and starting as discussed *supra*) the reading, writing, or transmission of data. (See D2, D3; ‘109 patent, col. 8, l. 51 to col. 9, l. 10.) As such, skilled artisans would have understood, in light of the ‘109 patent, the plain meaning of “signal” (see IEEE Dictionary definition cited *supra*), and other factors noted here, that the broad phrases recited in claims 7, 14, and 25 reasonably correspond to either of the prior art block size information or terminate signal systems, both of which tell the memory device when to end transmission.

Based on the foregoing discussion, the rejection of independent claims 7, 14, and 25, and dependent claims 8, 9, 15 and 16, argued together with these independent claims (see App. Br. 20), is sustained.

#### *Double Patenting*

The Examiner reasons that “the question is whether claim 1 of the instant patent is anticipated by claim(s) of the ‘037 patent.” (RAN 11.) The Examiner refers to claims 1, 7, 8, 10, and 11 of the ‘037 patent as the basis for the double patenting rejection, based on a theory of anticipation by these claims. (RAN 10-12, 39-40.) The Examiner’s theory appears to rely on the implicit existence of a delay value in claim 1 of the ‘109 patent. According

Appeal 2011-005255  
Reexamination Control 95/001,166  
Patent 7,287,109

to the Examiner, claim 1 specifies sampling after a number of clock cycles, and claim 7, which depends from claim 1, shows that the number is programmable. Therefore, according to the Examiner, this programmed number constitutes the signal recited in claim 1. (Claim 10, which depends from claim 1, and claim 11, which depends from claim 10, recite limitations similar to claim 7.)

But claim 1 in the '109 patent, in addition to reciting "providing a signal," also requires providing write data during even and odd phases of a "clock signal." The Examiner relies on Farmwald claim 8, which depends from claim 1, for these limitations. (RAN 39-40.)

Therefore, the Examiner's theory relies on a combination of Farmwald claims 7 and 8, both of which separately depend from claim 1, to show anticipation of the '109 patent claim 1. As Appellant argues (App. Br. 19), this reliance on two dependent claims (which do not depend on each other) means that no single claim in Farmwald anticipates claim 1 of the '109 patent.

Farmwald claim 8 does not specifically recite a "signal" apart from a "clock signal." Contrary to the Examiner's analysis that Farmwald claim 7 inherently or implicitly shows in claim 1, a programmable clock signal which in turn implies another (delay value) "signal" (*see* Ans. 11-12), the recitation of a programmable clock signal in dependent claim 7 shows the opposite, i.e., independent claim 1 does not necessarily require a programmable clock. For example, the number of clock cycles in claim 1 could be a fixed value, hard-wired or otherwise. It follows, according to the Examiner's rationale, that Farmwald claim 1/8 does not require both a "signal" and a "clock signal." In other words, the Examiner does not appear

Appeal 2011-005255  
Reexamination Control 95/001,166  
Patent 7,287,109

to interpret a fixed (i.e., non-programmable) clock signal as recited in Farmwald claim 1/8 to imply a separate signal as required by claim 1 in the '109 patent. (*See also* Ans. 41-44 (discussing claim construction).)

Pursuant to the foregoing discussion, the Examiner's obviousness-type double patenting rejection of claim 1 based on a theory of claim anticipation is in err. The RAN does not set forth an obviousness rationale for the double patenting rejection (e.g., articulating a reason to combine Farmwald's claims 7 and 8) so that such a rejection is not before us.

As such, the Examiner's double patenting rejection of independent claim 1 and claim 24 of similar scope to claim 1 is not sustained. The double patenting rejection of claims 2-6, 11-13, and 21-24 also is not sustained because these claims depend from claims 1 or 24 and the Examiner's rejection does not cure the above-noted deficiency in claim 8. (*See* RAN 40.)

#### Non-Adopted Rejections

Affirmance of the anticipation rejection for all claims based on Farmwald renders it unnecessary to reach the propriety of the Examiner's decision to refuse to adopt Requestor's remaining proposed rejections. *Cf. In re Gleave*, 560 F.3d 1331, 1338 (Fed. Cir. 2009) (not reaching obviousness after finding anticipation).

#### CONCLUSION

Farmwald anticipates claims 1-25.

#### DECISION

The Examiner's decision to reject appealed claims 1-25 is affirmed.

Appeal 2011-005255  
Reexamination Control 95/001,166  
Patent 7,287,109

Requests for extensions of time in this inter partes reexamination proceeding are governed by 37 C.F.R. § 1.956. *See* 37 C.F.R. § 41.79.

AFFIRMED

ak

Sterne, Kessler, Goldstein & Fox, PLLC  
1100 New York Avenue, NW  
Washington, DC 20005

Third Party Requester:

Haynes and Boone, LLP  
2323 Victory Avenue  
Suite 700  
Dallas, TX 75219