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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Inter Partes
NVIDIA, CORP.
Requestor, Appellant
v.

RAMBUS, INC.
Patent Owner, Respondent

Appeal 2011-005266
Reexamination Control No. 95/001,178
United States Patent 6,470,405 B2
Technology Center 3900

Before ALLEN R. MacDONALD, KARL D. EASTHOM, and
STEPHEN C. SIU, *Administrative Patent Judges*.

EASTHOM, *Administrative Patent Judge*.

DECISION ON APPEAL

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This proceeding arose from NVIDIA's request for an *inter partes* reexamination of the Rambus's patent, U.S. 6,470,405 to Barth et al., *Protocol For Communication with Dynamic Memory* (Oct. 22, 2002). Appellant, third-party Requestor NVIDIA, appeals under 35 U.S.C. §§ 134(b) and 306 from the Examiner's Right of Appeal Notice (RAN) confirming claims 1-37 of the '405 patent. Respondent, Rambus, supports the Examiner's decision. We have jurisdiction under 35 U.S.C. 35 U.S.C. §§ 6, 134, and 315.

We REVERSE.

STATEMENT OF THE CASE

Appellant and Respondent refer to several related judicial and other proceedings including *inter partes* and *ex parte* reexaminations, International Trade Commission proceedings, and Federal District Court and Circuit Court proceedings in their briefs. (App. Br. 3; Resp. Br. 4.) An oral hearing of this appeal, and related appeal, 2011-005255, concurrently transpired on May 4, 2011 and was transcribed on June 16, 2011.

The disputes on appeal primarily involve the control of a "memory device" via an "external strobe signal" as recited in the independent claims. (Claims 1, 11, 19, and 29.) Patent owner, Rambus, contends that the prior art does not teach or suggest sending a strobe signal to a DRAM, a dynamic random access memory chip, covered by a "memory device" according to the independent claims. (*See e.g.*, Resp. Br. 10-11.) The Examiner primarily agrees with Rambus, but Appellant, Requestor, NVIDIA, does not. The parties do not dispute that it was known to send strobe signals to a

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memory controller or to a memory stick. (*See e.g.*, Ans. 11-13, 17-20 (summarizing Appellant's and Respondent's positions).) A memory stick, according to another patent owned by Rambus, the Farmwald '755 patent, has at least one transceiver chip and at least one DRAM chip on a circuit board. (FW 6 *infra.*) A brief summary of the '405 patent (under reexamination) disclosure follows.

The '405 Patent (Factual Findings)

P1. The '405 patent discloses at least two embodiments, a strobe embodiment (col. 10, ll. 34-44) and a non-strobe, or variable delay value embodiment, (col. 10, ll. 45-60) for operating a memory device. Both embodiments employ a DRAM (dynamic random access memory) memory device (*see* col. 1, ll. 14-17) 603 having control logic 1910, control registers 614, internal clock 618, receiver 620, transmitter 616, DRAM memory core arrays 602, 606, and caches 604, 606. An external memory controller 601 sends request packets and other control information, including the strobe signal, to the DRAM 603. (*See* Fig. 6; col. 5, l. 28 to col. 8, l. 11.)

P2. In other words, the first embodiment employs a strobe signal while the second does not. In both embodiments, a memory device receives command control information causing it to begin a process for receiving data to be written to it or for transferring data from it. (Col. 9, ll. 20-45; col. 10, ll. 21-60.)

P3. In the first embodiment, the strobe embodiment, if the command control information specifies: 1) A write mode, the strobe signal subsequently causes the memory device to accept data from a data bus (i.e., for writing it into the memory device); 2) A read mode, the strobe signal subsequently causes the memory device to transfer data from the

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memory device control registers to the bus (i.e., after having prefetched data from the DRAM memory core pursuant to the command control information). (*See id.* and col. 7, ll. 41-45; Fig. 8.) The strobe signal causes the transfer to occur after several clock cycles. (*See e.g.*, Figs. 12, 13, Table at cols. 25-26 (indicating various delays in terms of clock cycles between the strobe and data transfer).) The system minimizes latency “[b]ecause the initial data packet to be transmitted by the DRAM has been prefetched from the core, [so that] the data packet can be transmitted over the channel with minimal delay from when the strobe signal ultimately arrives.” (Col. 9, ll. 32-35.)

The Claims

Exemplary claims 1 and 11 of the ‘405 patent under reexamination follow:

1. A method of operation in a semiconductor memory device, wherein the memory device receives an external clock signal and includes an array of memory cells, the method comprises:

receiving a first code synchronously with respect to the external clock signal, wherein the first code specifies that a write operation is to be initiated in the memory device receiving a second code synchronously with respect to the external clock signal, wherein the second code specifies that a precharge operation is to be initiated automatically after initiation of the write operation;

detecting an external strobe signal, wherein the external strobe signal indicates when to begin sampling data; sampling the data upon detection of the external strobe signal, wherein during the write operation, the memory device writes the data to the array; and

initiating the precharge operation automatically after the write operation is initiated.

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11. A method of controlling a semiconductor memory device, wherein the memory device includes an array of memory cells, the method comprises:

providing a plurality of control codes to the memory device wherein the plurality of control codes include a first code which specifies that a write operation be initiated in the memory device and a second code which specifies that a precharge operation be initiated automatically after initiation of the write operation;

delaying for an amount of time after providing the plurality of control codes; and issuing an external strobe signal to the memory device after delaying for the amount of time, to signal the memory device to sample data, wherein the data is to be written to the array during the write operation.

Requestor's Proposed Rejections

The Examiner did not maintain the following proposed rejections by Requestor:

Claims 11, 15, 16 and 18 as rejected for obviousness-type double patenting based on Farmwald et al., U.S. Patent 6,584,037 B2 (June 24, 2003, effectively filed April 4, 1990) (Farmwald '037").

Claims 11, 15, and 18 as anticipated under 35 U.S.C. § 102(e) by Watanabe et al., EP 0605887 B1 (Sept. 26, 2001) ("Watanabe").

Claims 11, 15, 16, and 18 as anticipated under 35 U.S.C. § 102(e) by Farmwald '037.

Claims 1, 2, 5-7, 10, 11, 14, 15, 18-20, 24, 25 and 27-32 as obvious under 35 U.S.C. § 103(a) based on Watanabe and Hayes et al., U.S. Patent 5,218,684 (June 8, 1993) ("Hayes").

Claims 3, 4, 12, 13, 21-23, 33, and 34 as obvious under 35 U.S.C. § 103(a) based on Watanabe, Hayes, and Inagaki, JP 57-210495 (Dec. 24, 1982).

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Claims 1-13, 15, 16, 18-22, and 24-35 as obvious under 35 U.S.C. § 103(a) based on Farmwald et al., U.S. Patent 5,319,755 (June 7, 1994, effectively filed April 18, 1990) (“Farmwald ‘755”) and Lu et al., *The Future of DRAMs*, 1988 IEEE Intern. Solid-State Circuits Conf. (ISSCC), Digest of Tech. Papers, pp. 98-99 (Feb. 1988) (“Lu”).

Claims 1-13, 15, 16, 18-22, and 24-35 as obviousness under 35 U.S.C. § 103(a) based on Farmwald ‘755 and *Memory Components Handbook*, Intel. Corp., Ch. 1, 3 (1985)(“iRAM”).

Claims 17, 36, and 37 as obvious under 35 U.S.C. § 103(a) based on Farmwald ‘755, Lu, and Kushiyama et al., *A 500-Megabyte/s Data-Rate 4.5M DRAM*, IEEE J. Solid State Circuits, V. 28, No. 4, pp. 490-98 (Apr. 1993) (“Kushiyama”).

Claims 3, 4, 12, 13, 21-23, 33, and 34 as obvious under 35 U.S.C. § 103(a) over Barth et al., U.S. Patent 5,748,914 (May 5, 1998, filed Oct. 19, 1995) (“Barth”) and Kushiyama.

(See App. Br. 6.)

ISSUES

As the analysis below shows, the Briefs and Answer raise the following issues:

Does Watanabe disclose issuing a strobe signal as recited in independent claim 11?

Would it have been obvious to employ Hayes’s strobe signal with Watanabe’s semiconductor memory device, rendering obvious independent claims 1, 11, 19, and 29?

Does the combination of Farmwald ‘755 and either Lu or iRAM render obvious the use of a strobe signal in a synchronous memory device as recited in the independent claims 1, 11, 19, and 29?

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Did the Examiner err by failing to maintain the rejection of claims 3, 4, 12, 13, 21-23, 33, and 34 for obviousness based on the combination of Watanabe, Hayes, and Inagaki?

Did the Examiner err by failing to maintain the rejection of claims 17, 36, and 37 for obviousness based on the combination of Farmwald '755, Lu, and Kushiyama as proposed by Requestor?

PRINCIPLES OF LAW

Claims “must be read in view of the specification. . . . [T]he specification ‘is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.’” *Phillips v. AWH Corp.*, 415 F.3d 1303, 1315 (Fed. Cir. 2005) (en banc) (citation omitted).

“Even when the specification describes only a single embodiment, the claims of the patent will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using ‘words of manifest exclusion or restriction’.” *Leibel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004) (citation omitted). “Indeed, a claim interpretation that would exclude the inventor’s device is rarely the correct interpretation; such an interpretation requires highly persuasive evidentiary support” *Modine Mfg. Co. v. U.S. Intern. Trade Comm’n*, 75 F.3d 1545, 1550 (Fed. Cir. 1996) (cited with approval by *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1583) (Fed. Cir. 1996)).

ANALYSIS

Watanabe – Anticipation of Claims 11, 15, and 18

Appellant maintains that Watanabe’s external clock signal reads on the “strobe signal” recited in independent claim 11. (*See* App. Br. 7-10.) Respondent maintains that the ‘405 patent clearly distinguishes between “the number of clock cycles . . . and . . . the strobe signal.” (Resp. Br. 8 (quoting the ‘405 patent at col. 10, ll. 39-49).) Respondent also points out how the strobe signal and clock signal are distinct by relying on Figures 12 and 13 of the ‘405 patent (*id.* at 7-8) and Respondent’s expert testimony to “show that “a ‘strobe signal’ [, unlike a clock signal,] is a signal that is asserted only when needed to perform specific functions” (*id.* at 9 (citing Murphy Decl. at ¶30, ¶¶ 21-31).) The Examiner agrees with Respondent and reasons that a clock signal, unlike a strobe signal, is periodic. (Ans. 5-6 (citing Murphy Decl. at ¶ 27).)

Respondent’s and the Examiner’s claim interpretation is more persuasive because, in light of the ‘405 patent, the clock signal and strobe signal are distinctly different. (*Accord* P2-P3.) As such, the Examiner did not err in not maintaining the proposed anticipation rejection of claims 11, 15, and 18 based on Watanabe.

Watanabe with Hayes – Obviousness of

Claims 1, 2, 5-7, 10, 11, 14, 15, 18-20, 24, 25, and 27-32

Requestor’s (Appellant’s) proposed rejection involves combining an asserted strobe signal from Hayes as a functional addition to the memory device, or chip, of Watanabe. (App. Br. 10-14.) Respondent maintains that the Examiner properly found that this proposed combination would not have been obvious. (Resp. Br. 10-11.)

Additional Findings of Fact

Watanabe

W. Watanabe discloses a “synchronous LSE memory device” and clock signal (¶¶ 0017, 0019) and states that the term “latency” is widely known as “when a command is inputted and when data are transferred in a synchronous device” (¶0018).

Hayes

H1. For a write cycle, “[t]he bus master . . . drives data onto DAL [31:0] . . . and asserts DS [data strobe col. 7, l. 56], indicating that the data is valid on DAL [31:0]. If no error occurs, the slave device reads the data, and the external logic asserts RDY. If an error occurs, external logic asserts ERR, which aborts the bus cycle.” (Col. 9, ll. 56-63.)

H2. External logic asserts the ERR function “whenever a parity error occurs on a read from a local RAM 13, provided that parity is enabled” (Col. 11, ll. 33-35). The ERR function indicates “the abnormal termination of a read, write or interrupt acknowledge cycle.” (Col. 8, ll. 9-11.)

H3. Hayes provides bus cycles with read and write cycles (col. 7, ll. 20-27; and the processor “synchronizes an IRQ signal internally” (col. 8, ll. 53-54). “A CPU read cycle lasts at least eight clock phases” (*id.* at col. 9, ll. 33-36) as does a write cycle (*id.* at ll. 49-53). During the write cycle, the bus master drives an address onto DAL (data and address lines) and outputs data to memory. (*Id.* at 49-55.)

Discussion

The arguments focus on independent claim 1, hereby selected to represent the group of claims listed under the heading *supra*. (See App. Br. 10-14; Resp. Br. 10-11.) Appellant contends that the Examiner erred by

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failing to maintain the proposed rejection which combines the functionality of Hayes's strobe signal with Watanabe's system, where both systems write data after waiting for delays defined by latency values. (*See* App. Br. 10-12.) Respondent contends that the proposed combination would not have been obvious "because Hayes is asynchronous, it uses a different communication and data transfer protocol that is not adaptable to the synchronous system described in Watanabe." (Resp. Br. 10 (citing Murphy Decl. ¶ 89).) Respondent also maintains that older asynchronous systems like that of Hayes do not have "a clock analogous to Watanabe's CLK that controls the overall timing of memory device operations," and skilled artisans would not have employed a logic signal provided to a logic device which controls seventy-two asynchronous DRAM memory devices as occurs in Hayes, and supply it directly to the DRAM described in Watanabe. (Resp. Br. 10; citing Murphy Decl. ¶¶ 87-90.)¹

Appellant's expert, Mr. Parris, partly in response to the Murphy Declaration (Parris Decl. ¶ 1 (attached as App. Br. Ex. 27)), testifies that skilled artisans in the semiconductor DRAM industry, including himself, were transitioning to newer synchronous systems in part by "incorporat[ing]

¹ Respondent's arguments parallel Mr. Murphy's testimony which also states that "no one would have taken a back-plane signal such as [Hayes's] DS that is provided to a memory control logic device on an asynchronous memory array board, and supplied it directly to the asynchronous memory device described in Watanabe." (Murphy Decl. ¶ 90 (attached as Exhibit 10 to Respondent's Brief).) It is not clear here if Mr. Murphy intended to refer to "asynchronous" memory devices in Watanabe or if this is a typographical error and Mr. Murphy intended to use the word "synchronous." In any event, Watanabe discloses a synchronous memory device (W), and Respondent does not specifically argue that Watanabe fails to disclose a synchronous memory system or device (*see* Resp. Br. 10).

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asynchronous functionality that had existed on previous asynchronous memory systems into synchronous memory systems” (Parris Decl. ¶ 9).

Mr. Paris generally explains that the newer synchronous DRAMs incorporated more logic, registers, latches, and associated functions all on-chip - thereby making the devices faster by reducing propagation delays (by shortening the propagation distance between circuit locations). (*See id.* at ¶¶ 9, 12 (citing Farmwald ‘755 and Lu’s *Future of Drams* article), 17 (converting from asynchronous to synchronous increases speed), 18 (describing Hayes), 19 (asserting that Mr. Murphy (citing Murphy Decl. at ¶¶ 79-82) does not provide a reason for asserting that providing on-chip logic reduces speed)), 23.) Mr. Paris also refers to such modifications as “straight forward and well within the ability of one of ordinary skill in the art.” (*Id.* at ¶ 9; *accord* ¶ 23.)² Mr. Paris’s testimony is corroborated by the Farmwald ‘755 patent and other references of record. (*See* FW3, FW5 (detailing similar on-chip logic changes as involving ordinary skill); Lu; and iRAM (both discussed *infra*.)

Appellant also explains that Watanabe and Hayes both employ systems for handling latency, with Hayes using a data strobe signal to indicate when valid data is on a bus, and with Watanabe employing a synchronous clock system to handle latency. (*See* App. Br. 12-13.)

Appellant also maintains that the combination involves use of a known technique to improve similar devices in the same way. (*Id.* at 13.)

² Mr. Paris explains states that during the 1980s and up until 1995 most DRAMs were asynchronous, and thereafter, “most new designs were synchronous.” (Paris Decl. ¶ 9.) In general, according to Mr. Parris, employing an external clock to control different devices and logic in a system renders the system synchronous. (*Id.*)

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The Examiner (analyzing anticipation), agrees that Watanabe discusses latency (*see* Ans. 8), “agrees that a DS signal could possibly be applied to the system of Watanabe” (Ans. 13), and also agrees that “a synchronous memory device does not exclude signals which may be asynchronous” (*id.*). The Examiner also finds that “Watanabe discloses . . . a DRAM chip . . . [and] hence this is the chip that must receive the strobe signal” of Hayes. (Ans. 11.) Nonetheless, the Examiner reasons that it would not have been obvious to send Hayes’s DS strobe signal to Watanabe’s chip because the DS signal “is not received by the memory device” in Hayes. (Ans. 11.)

On balance, Appellant’s arguments, supported by Mr. Parris, are more persuasive than the rationale provided by the Examiner and Respondent. The latter rationale improperly attacks the references separately. Respondent and the Examiner do not address Appellant’s arguments which tend to show that the two memory systems (in Watanabe and in Hayes) both deal with reading and writing data to memory devices while accounting for latency (i.e., the time required to perform reads and writes, retrieve data, etc. (*see e.g.*, W; P3)). Respondent and the Examiner also do not rebut Mr. Paris’s testimony describing how known asynchronous functions were being combined routinely with, and integrated into, synchronous DRAM systems by skilled artisans.

Based on Appellant’s arguments and the evidence of record, the proposed modification, i.e., using Hayes’s DS (data strobe) method of controlling latency to supplement Watanabe’s method of controlling latency, would have amounted to using a known function for its intended purpose on a similar device. The evidence also shows that skilled artisans were

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routinely making similar adjustments. Respondent's arguments and evidence based on Mr. Murphy's declaration, show at most that incorporating all the logic hardware and functionality from Hayes's RAM CONTROL LOGIC 62 onto Watanabe's DRAM(s) to control this timing would have been unobvious as producing unworkable chips with reduced speed. (See Resp. Br. 10; Murphy Decl. at ¶¶ 79-82). In other words, Respondent's arguments, alleging the unobviousness of incorporating Hayes's *complete* logic system into Watanabe's DRAM, fail to show how incorporating Hayes's *singular* DS function with Watanabe's DRAM would have been unobvious.

Respondent also contends that Hayes's data strobe signal (DS) does not operate according to the claimed strobe signal. (Resp. Br. 11.) This contention is not persuasive. The DS signal, a "data strobe" signal (H1), reasonably indicates that data is valid on the data lines as Appellant maintains. (App. Br. 12 (quoting Hayes at col. 9, ll. 49-60); *accord* H1.) Respondent's argument and the Examiner's similar rationale (Resp. Br. 11-12; Ans. 11-13) that Hayes does not employ the DS signal on a "memory device," but instead, sends it to an external controller, i.e., the RAM CONTROL LOGIC 62 (Resp. Br. 11), improperly attacks the references separately, as indicated above. The Examiner also agrees that Hayes's DS signal could be applied to Watanabe's DRAM as noted *supra*. As such, the arguments and rationale fail to rebut Requestor's proposed obviousness rejection based on the combination – i.e., integrating Hayes's DS logic into Watanabe's DRAM and strobing the DRAM would have been obvious to account for latency by indicating that data is ready for reading or writing.

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Respondent's related assertion that data is not sampled until after an error check is completed in Hayes is not persuasive for several reasons. (Resp. Br. 11.) (The Examiner does not appear to adopt this position.) The "ERR" signal in Hayes occurs after the DS signal as Respondent indicates. (H1, H2.) However, Requestor's proposed rejection does not seek to incorporate this separate ERR function with the DS signal function. In addition, external logic asserts the ERR function "whenever a parity error occurs on a read from a local RAM 18, *provided that parity is enabled*" (H2 (emphasis supplied).) In other words, in Hayes, this ERR function appears to be a mere option because it may or may not be enabled in a particular system. Moreover, it only occurs to show an "abnormal" termination of a read, write, or interrupt. (H2.) As such, since claim 1 does not require immediate action based on the strobe signal, claim 1 does not preclude infrequent (abnormal) interrupts by this ERR system, and even if it does, as just explained, Hayes teaches that this ERR function is optional and thereby separate from the DS signal.

Finally, contrary to Respondent's assertions noted *supra*, Hayes does employ at least one external clock, and also provides synchronization, at least with respect to an internal clock. (H3.) Such clocking and synchronization further suggests the combination of Hayes DS signal with Watanabe's synchronized system.

For the foregoing reasons, the Examiner erred by not maintaining Requestor's proposed obviousness rejection of claim 1 based on the combination of Watanabe and Hayes. Respondent argues that claims 11, 19, and 29 recite similar features to those disputed in claim 1. (Resp. Br. 11.) Respondent does not offer separate reasons in support of the

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Examiner's decision to decline maintaining Requestor's proposed rejection of claims 2, 5-7, 10, 11, 14, 15, 18-20, 24, 25, and 27-32. The Examiner similarly groups the claims together in the Answer and does not provide separate reasons for refusing to maintain the proposed rejection. (Ans. 11-13.) Therefore, based on the arguments and findings presented here, the Examiner also erred by not maintaining the rejection of these claims as Requestor proposed.

Watanabe, Hayes, and Inagaki

Obviousness of claims 3,4, 12, 13, 21-23, 33 and 34

The Examiner confirms patentability of these claims based on the confirmed patentability of claim 1 over the combination of Watanabe and Hayes. (Ans. 14.) Respondent relies on this confirmed patentability, and also asserts that while Inagaki uses the term "clock," the signals relied upon by Appellant "are merely pulsed control signals" as opposed to periodic signals, and as such, "Inagaki cannot teach using both an even and odd phase of an external clock." (Resp. Br. 12 (citing Murphy Decl. at ¶ 132); *accord* Resp. Br. 13 (quoting Inagaki at 5 as disclosing "'clocks ϕ_1 and ϕ_2 '" and providing a copy of Inagaki's Figure 4, and citing Murphy Decl. at ¶¶ 126-132).)

Appellant refers the Board to the proposed rejection at Exhibit K of the (original) Request for a "[d]etailed analysis" of how the claims read on the combined teachings. (App. Br. 14). Respondent maintains that this reference to the request is improper (as not included in the Brief). (Resp. Br. 12 (citing 37 C.F.R. § 41.67(c)(1)(vii) and *Ex parte Flemming*, 2009-005123 (BPAI 2010) (non-precedential)).)

Additional Findings of Fact

Inagaki

I1. “The rise and fall of external clock ϕ are detected, and clocks ϕ_1 and ϕ_2 are generated. Clocks ϕ_1 and ϕ_2 drive shift pulses of the shift register. . . . [T]he operating speed is twice that of the conventional speed.” (Inagaki 4).

I2 “[T]he present invention presents block access memory that transfers data with a speed that is twice the conventional speed, by performing I/O [input/output] of data on every half-cycle of the external clock that drives the I/O shift register.” (*Id.* at 3.)

Discussion

Respondent’s arguments and Mr. Murphy’s Declaration are directly contradicted by Inagaki which recites an “external clock ϕ ” generating “clocks ϕ_1 and ϕ_2 .” (I1.) Respondent quotes, *inter alia*, the portions I1 and I2 at Exhibit K of the Request in detailing the proposed rejection. The proposed rejection constitutes a prima facie rejection which Respondent’s arguments fail to rebut. Contrary to Respondent’s argument outlined *supra*, neither the cited Board opinion (which relies on Bd .R. 41.67, *id.* at 3, n.1), nor the cited rule, requires Requestor’s proposed rejections to be repeated in a Brief.

Turning back to the merits, Mr. Murphy’s basis for concluding the clock is merely an aperiodic pulse generator appears to be founded on an assertion that Figure 4 only shows two clock pulses and that Inagaki’s shift registers “*operate on shift pulses according to clocks ϕ_1 and ϕ_2 .*” (Murphy Dec. ¶ 132 (emphasis by Mr. Murphy, quoting Inagaki at 5.)) This statement does not support Respondent’s position because it refers to the

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clocks as “clocks,” not pulses, and it indicates that registers operate on shift pulses which are generated according to the clocks. Another portion of Inagaki verifies that the clocks drive shift pulses. (I1.) Figure 4 only shows a portion of the clock cycles; based on the description of clocks and half-cycles (I1, I2), skilled artisans would not have concluded from a failure to display repeated clock cycles that the clock is not periodic. As Mr. Murphy states: “[The translation of Inagaki . . . uses the work ‘clock’ in numerous locations” (Murphy Dec. ¶ 129.)

Respondent also contends that Inagaki’s clock signal is not external and that “there is no motivation to use the alleged clocking scheme of Inagaki with Watanabe” because “like Hayes, Inagaki describes an asynchronous system.” (Resp. Br. 13.) These arguments also lack merit partly for reasons stated above (i.e., asynchronous to synchronous migration was well-known), and also because Inagaki clearly discloses an “external clock ϕ ” (I1) having odd and even phases (i.e., on rising and falling edges of the external clock (Inagaki Fig. 6; I1)) which in turn generate clock phases “to transfer data with . . . twice the conventional speed” (I2). (*Accord* Request, Ex. K (detailing the rejection of claims 3 and 4).) Respondent’s arguments do not show why this “universal” desire for “faster” operations, i.e., an “implicit motivation,” would have been isolated to asynchronous devices. *Dystar Textilfarben GmbH & Co. Dutschland KG v. C.H. Patrick Co.*, 464 F.3d 1356, 1368 (Fed. Cir. 2006) (“[A]n implicit motivation to combine exists . . . when the ‘improvement’ is technology-independent and the combination of references results in a product or process that is more desirable, for example because it is stronger, cheaper, cleaner, faster, lighter, smaller, more durable, or more efficient.”)

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Based on the foregoing discussion, the Examiner erred by failing to maintain Requestor's proposed rejection of claims 3, 4, 12, 13, 21-23, 33, and 34.

Farmwald '755 with either of Lu or iRAM
Obviousness of Claims 1-13, 15,16, 18-22 and 24-35

The arguments here raise issues which are similar to the issues addressed *supra*. Primarily, the parties dispute whether or not Farmwald '755, in view of either Lu or iRAM, renders obvious sending a strobe signal to a "memory device" as required by the independent claims at issue. The parties agree that Farmwald '755 at least sends a strobe signal, called the TrncvrRW signal in Farmwald '755, to a memory stick. (*See Ans. 18-19.*)

Additional Findings of Fact

Farmwald '755

FW1. Farmwald employs a master/slave bus-based system. A master gives "each device on the bus a unique device identifier (device ID)" (col. 15, ll. 23-24) and uses the identifier to access a specific device. "[E]ach device connected to the bus contains a special device-type register which specifies the type of device, for instance CPU, 4 MBit memory, 64 MBit memory or disk controller." (Col. 15, ll. 33-36.) Masters also send request packets and detect collisions for bus arbitration. (Col. 13, ll. 7-12; col. 14, ll. 52-61.)

FW2. The disclosed invention saves power by performing a row access on a "single RAM to supply all the bits for a block request (compared to a row-access in each of multiple RAMs in conventional memory systems) [and thus] the power per bit can be made very small." (Col. 18, ll. 9-12.)

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Such reduced power allows RAMs to be stacked and/or placed closer together than RAMs in the prior art. (Col. 18, ll.13-15, ll. 45-49.)

FW3. The invention also provides for a multiplexed time shared bus on a small number of bus lines. Therefore, the number of pins per device, even for an “arbitrarily large memory device[,] can be kept quite small – on the order of 20 pins [, and] kept constant from one generation of DRAM density to the next.” (Col. 18, ll. 20-23.)

FW4. The time delay for writing a block of data to the data lines occurs via an op code transmitted in a request packet to a slave device such as a DRAM. The code either directly specifies a register in the DRAM which holds the delay value or the DRAM indirectly responds to the codes with preselected access times (apparently via a table). (See col. 9, l. 27 to col. 10, l. 17.)

FW5. The DRAMs in Farmwald are described as differ[ent] from conventional DRAMs in a number of ways. Registers are provided which may store control information, device identification, device-type and other information appropriate for the chip such as the address range for each independent portion of the device. New bus interfaces circuits must be addressed and the internals of prior art DRAM devices need to be modified so they can provide and accept data to and from the bus at the peak data rate of the bus. This requires changes to the column access circuitry in the DRAM, with only a minimal increase in die size. A circuit is provided to generate a low skew internal device clock for devices on the bus, and other circuits provide for demultiplexing input and multiplexing output signals.
(Col. 4, ll. 21-35.)

FW6. Farmwald teaches that up to about 32 of the above-described DRAMs can be used on the bus while maintaining speed. If more memory

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is required, another device can be used, a memory stick, also called a primary bus unit (*see* Fig. 9), which itself can carry up to about 32 such DRAMs on the stick (i.e., a circuit board), and the memory system can employ multiple memory sticks. Each memory stick includes a transceiver in addition to one or more of such DRAMs, all connected on a primary bus. Each memory stick, with its primary bus of DRAMs, then connects via the transceiver device to a larger system bus, called a transceiver bus. (Col. 20, l. 48 to col. 21, l. 17; col. 22, ll. 1-31.)

“The transceivers are quite simple in function. They detect request packets on the transceiver bus and transmit them to their primary bus unit.” (Col. 21, ll. 18-20.)

FW7. Farmwald ‘755 refers to a “memory device,” a “transceiver device” and “peripheral devices” as follows:

In a preferred implementation, all masters are situated on the transceiver bus so there are no transceiver delays between masters and all memory devices are on primary bus units so that all memory accesses experience an equivalent transceiver delay, *but persons skilled in the art will recognize how to implement systems which have masters on more than one bus unit and memory devices on the transceiver bus as well as on primary bus units. In general, each teaching of this invention which refers to a memory device can be practiced using a transceiver device and one or more memory devices on an attached primary bus unit.* Other devices, generically referred to as peripheral devices, including disk controllers, video controllers or I/O devices can also be attached to either the transceiver bus or a primary bus unit as desired.
(Col. 20, l. 67 to col. 21, l. 14 (emphasis added).)

FW8. The system uses a TrncvrRW signal to control writing and reading as follows:

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Persons skilled in the art will recognize that a more sophisticated transceiver can control transmissions to and from primary bus units. An additional control line, TrncvrRW can be bused to all devices on the transceiver bus, using that line in conjunction with the Addr-Valid line to indicate to all devices on the transceiver bus that the information on the data lines is 1) a request packet, 2) valid data to a slave, 3) valid data from a slave, or 4) invalid data (or idle bus). Using this extra control line obviates the need for the transceivers to keep track of when data needs to be forwarded from its primary bus to the transceiver bus – all transceivers send all data from their primary bus to the transceiver bus whenever the control signal indicates the condition 2) above.

(Col. 21, ll. 35-49 (emphasis supplied).)

Farmwald' 755 discloses a “still more sophisticated receiver” (which only sends signals at requested times) in addition to the just-described transceiver. (Col. 21, ll. 65-68.)

FW9. Farmwald '755 describes device interfaces as follows:

The device interface to the high-speed bus can be divided into three main parts. The first part is the electrical interface. This part includes the input receivers, bus drivers, and clock generation circuitry. . . . The final part, specifically for *memory devices such as DRAMs*, is the DRAM column access path *Persons skilled in the art recognize how to modify prior-art address comparison circuitry and prior-art register circuitry in order to practice the invention.*

(Col. 22, ll. 34-52 (emphasis supplied).)

FW10. Circuitry which “is well-suited for use in DRAM devices . . . can be used or modified by one skilled in the art for use in other devices connected to the bus of this invention.” (Col. 22, ll. 57-61.)

Lu

L1. The Lu moderator predicts that “opportunities arise for incorporating complex on-chip logic functions to make DRAMs more intelligent.” (Lu 98, ¶ 1.) One of the Lu article panelists explains that

adding logic functions on-chip with the memory, provide high density and high performance in electronic systems. Data processing executed within one chip eliminates interface loss in speed and power consumption, which has been existing inevitably in combinations of standard DRAMs with basic common functions and logic parts.

(Lu 99, ¶ 1.)

Discussion

Requestor, Appellant, asserts that the strobe signal recited in the claims at issue here read on the TrncvrRW signal in Farmwald ‘755 (*see* FW8). (Request 38; App. Br. 17-18.) Neither the Examiner (*see* RAN 28; Ans. 17-18), nor Respondent (*see* Resp. Br. 16-20), dispute this assertion before the Board.

Rather, the Examiner and Respondent dispute Appellant’s contention that it would have been obvious to employ the TrncvrRW (i.e., strobe) signal as a signal to a memory device - as recited in the claims at issue. (Ans. 17-20; Resp. Br. 16-17.) Contrary to Respondent’s arguments and the Examiner’s findings, Farmwald ‘755, with or without Lu’s or iRAM’s teachings, at least renders obvious employing the TrncvrRW strobe signal to a “memory device” as recited in the claims at issue here.

Respondent acknowledges that Farmwald ’755 states that “TrncvrRW can be bused to all [] devices *on the transceiver bus*,” (Resp. Br. 16 (emphasis by Respondent, quoting Farmwald ‘755 at col. 21, ll. 37-43)), but Respondent argues that in Figure 9, “only the transceivers 19 are

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shown on that [transceiver] bus [65]” (Resp. Br. 17). Apparently, according to Respondent, by showing only transceivers as receiving the TrncvrRW signal in Figure 9, this amounts to teaching away from applying the TrncvrRW signal to a single memory device - as the Examiner also found. (See Resp. Br. 17-18 (citing and discussing the RAN.) Respondent also maintains that Appellant failed to respond to the Examiner’s teaching away finding, thereby waiving the issue. (Resp. Br. 16.)

There is no dispute that Farmwald ‘755 discloses at least two embodiments, a single-chip DRAM device (Fig. 2), and a primary bus unit – also described as a transceiver/memory stick device (Fig. 9). (See App. Br. 17; Resp. Br. 17; *accord* FW6.) This memory stick includes at least one DRAM and a transceiver. (FW6; FW7; *accord* Resp. Br. 19; Ans. 20.) By arguing that only transceivers are on the transceiver bus, Respondent is effectively arguing that the phrase quoted *supra* from the ‘755 patent, “all devices on the transceiver bus” (FW8 (emphasis added)), refers only to transceiver devices. But the ‘755 patent directly contradicts this view by referring to “memory devices on the transceiver bus as well as on primary bus units” (FW 7).) (Rambus asserts that the memory stick is not a memory device in a related reexamination now on appeal to the Federal Circuit, Appeal No. 2010-0011178, Reexam. No. 90/010420.)³

³ The Board held in Appeal No. ‘178 that the memory stick embodiment disclosed in the patent under reexamination there is a memory device. All of the independent claims here similarly recite a “memory device,” and additionally, all, except for claim 20, recite a “semiconductor memory device” in the respective preambles. While Requestor contends that a memory device need not be a single chip, Requestor raises this issue in a Rebuttal Brief – though it has been raised in related proceedings based on applications bearing “the exact same specification as the ‘405 patent.” (App.

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As such, Appellant’s argument is persuasive and supported by the record: The TrncvrRW signal indicates that “valid data to a slave” is available on the data bus, and that “[c]learly, a slave (e.g., a memory device should not begin sampling data from the bus if the data is not valid. Also . . . all devices on the bus receive the TrncvrRW signal, including the single-chip DRAM memory devices and the primary bus units.” (App. Br. 17-18.)

Farmwald ‘755 also specifically teaches that “*each teaching of this invention which refers to a memory device can be practiced using a transceiver device and one or more memory devices,*” i.e., can be practiced using a memory stick. (FW7.) Thus, even if Farmwald ‘755 does not anticipate the claims at issue here, skilled artisans would have recognized that teachings involving a single-chip (DRAM) memory device apply to transceiver devices and vice versa as Farmwald ‘755 indicates. (FW7; *see also* FW10 (showing that skilled artisans would have recognized that other devices on the bus can be modified similarly to DRAMs).)

The Examiner’s findings do not rebut Respondent’s contentions for obviousness. Specifically, the Examiner finds that “it is unknown whether the TrncvrRW signal will be used in other embodiments since Farmwald does not call the bus which is directly connected to the memory device a

Reb. Br. 4 n.4.) Appellant also states that in the context of Hayes, “[a] memory device need not be a single chip.” (App. Br. 11, n.5.) But it does not appear that Respondent proposed this rationale as part of the proposed rejection involving Farmwald ‘755 (or Hayes). Our rationale here, based on more clearly generated issues by the parties, allows us to decline to decide here whether or not a memory device is limited to a single (or a handful of) chip(s), or if a semiconductor memory device as recited in the preambles of (most of) the independent claims here limits the memory device to a single chip, or if Requestor timely raised the issue.

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transceiver bus. However, the Examiner acknowledges that both the transceiver bus and the primary bus is identical in electrical and other respects, however” (RAN 29; *accord* Ans. 17.)

The Examiner also points to arguments by Rambus and Respondent’s expert Mr. Murphy and concludes that Farmwald ‘755 teaches away from the claimed invention because the memory stick embodiment provides for chip expansion – i.e., allowing the number of chips on the stick to increase. (RAN 30 (citing Murphy Supp. Decl. ¶ 34).) The Examiner similarly reasons that “integrating the transceiver will remove all the benefits [i.e., chip expansion] associated with the transceiver” which shows teaching away. (Ans. 19.)

Based on the discussion above, this rationale fails to address the fact found *supra* that all memory devices in Farmwald ‘755 receive the strobe signal, TrncvrRW. Thus, by definition, Farmwald’ 755 cannot teach away as asserted. Assuming for the sake of argument that the finding of applying the strobe signal to all memory devices is not supported, the specific obviousness rationales are addressed more fully next.

1) Farmwald ‘755 and Lu

Contrary to the Examiner’s and Respondent’s (similar) rationales, even if memory sticks allow for chip expansion, this does not relate to the first dispute at issue here - Appellant’s proposed rationale for combining Farmwald ‘755 and Lu – i.e., whether or not applying the TrncvrRW signal to a memory device (i.e., a single chip) would have been obvious, as Appellant argues. (App. Br. 18.) In other words, Farmwald ‘755’s memory sticks have little to do with the proposed rejection, because they could have been expanded regardless of whether or not it would have been obvious to

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send the TrncvrRW signal directly to the single-chip devices disclosed in Farmwald '755. As Appellant similarly points out, one major benefit of the Farmwald '755 system is to allow different types of devices, including peripheral devices, DRAMs, and memory sticks, to attach to the bus. (Resp. Reb. Br. 6-7; FW1; FW7.) Farmwald '755 also indicates other goals for decreasing the power per pin while allowing for natural DRAM expansion in “an arbitrarily large memory device” (FW3). (*Accord* FW2.) Modifying a DRAM in the manner proposed does not defeat these goals including the goal of providing a memory stick (and such modifications were well within the skill in the art (*see e.g.* FW7, FW9, FW10, L1, Paris Decl.)).

As Appellant also points out, the TrncvrRW signal indicates valid data is ready for sampling (*id.*; *accord* FW8) such that “it would have been obvious for Farmwald’s single-chip DRAM device to also wait for the TrncvrRW . . . before it begins sampling data.” (App. Br. 18.) Still further, Farmwald '755 describes the TrncvrRW signal system as a more “sophisticated” method of control (FW8) – i.e., presumably more sophisticated in comparison to sending op codes in control packets which designate delay values directly or indirectly as described in previous sections of the patent (FW4). In other words, Farmwald '755 at least suggests applying this more sophisticated control method to the memory stick and single-chip devices.

As such, Respondent’s argument that the proposed combination defeat’s one of the goals in Farmwald '755: “to keep the intelligence concentrated in the masters, thus keeping the slaves [i.e., the memory devices] as simple as possible” (Resp. Br. 19 (quoting Farmwald’ 755 at col. 8, ll. 59-62) (bracketed information by Respondent)), is not persuasive.

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Farmwald '755 teaches modifying existing DRAMs (FW4, FW9, FW10) – thereby showing a trade-off to the asserted goal of simplicity in slaves, or at the least, showing that simplicity does not preclude modifications. Also, Farmwald '755 teaches “sophisticated” and “still more sophisticated” devices, thereby showing a similar trade-off at least in relation to transceivers. (FW8.) And Farmald '755 does not clearly define a transceiver (on a memory stick) as a master (*see* FW7), as masters have relatively complicated functions (FW1) and the transceiver devices are described as mere bus interfaces with relatively simple functions (FW 6). Thus, the record indicates that employing the TrncvrRW signal to a DRAM (and modifying the DRAM to accommodate such a signal) would not have rendered such a DRAM an overly complicated device. Further, Farmwald '755 indicates other important goals outlined *supra* (e.g., low power per pin, DRAM memory expansion, attachment of multiple devices to a small bus, etc.), none of which would have been compromised by sending a TrncvrRW signal to a DRAM. (*See* FW2, FW3.) As such, integrating strobe logic into a DRAM fails to defeat the asserted goals of keeping slaves simple or precluding memory expansion in memory sticks, and allows other goals to be met.

Appellant’s rationale reasonably shows that applying the TrncvrRW signal to the single-chip embodiment at least would have been obvious to ensure that valid data on the bus is ready for sampling, with the proposed rejection implicitly allowing for chip expansion on a memory stick. As such, the rationale teaches toward the claimed invention and constitutes a sufficient rebuttal of any asserted teaching away based on equivocation, simplicity, and chip expansion.

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To buttress this rationale, Appellant also quotes Lu to show that it would have been obvious to create “application specific (ASIC) DRAMs” (App. Br. 10) (quoting Lu at 99), because “adding logic functions on-chip with the memory[] provide[s] high density and high performance . . . within one chip [which] eliminates interface loss in speed and power consumption, which has been existing inevitably in combinations of standard DRAMs with basic common functions and logic parts.” (*Id.*; accord L1.) In other words, it would have been obvious to employ known memory stick functions in a single integrated DRAM package to increase speed and decrease power consumption. Farmwald ‘755 makes it clear that skilled artisans knew how to modify existing DRAM circuits and logic (FW9), and Farmwald specifically teaches modifying such DRAMs (FW1-3, FW5, FW10).

Respondent’s counter arguments that Lu is equivocal and teaches away from “moving logic on-chip” are not persuasive. Respondent, at most, demonstrates that Lu teaches tradeoffs in terms of “economics” versus “generic[]. . . benefits.” (Resp. Br. 18.) But the benefits of speed, reduced power (i.e., efficiency), and compactness constitute universal motivators “even absent any hint of suggestion in the references themselves.” *Dystar*, 464 F.3d at 1368 (“[A]n implicit motivation to combine exists . . . when the ‘improvement’ is technology-independent and the combination of references results in a product or process that is more desirable, for example because it is stronger, cheaper, cleaner, faster, lighter, smaller, more durable, or more efficient.”) “In such situations, the proper question is whether the ordinary artisan possesses knowledge and skills rendering him *capable* of combining the prior art references.” *Id.* Respondent does not point to sufficient

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evidence showing that skilled artisans were incapable of combining memory stick functions into a DRAM (which would have rendered the DRAM faster, smaller, and more durable than the memory stick).

Patent Owner states that Requestor proposes a new ground of rejection with respect to the “delaying for an amount of time” element as recited in claim 11. (Resp. Br. 17-18.) The discussion about this element is not clear and appears to relate to an alternative proposed rationale not related to the TrncvrRW embodiment discussed at length. (*See also* Ans. 18; App. Reb. Br. 7; App. Br. 18.) As such, finding of obviousness based on applying a TrncvrRW signal to a memory device renders the resolution of any dispute concerning this alternative rationale moot.

Based on the foregoing reasons, the Examiner erred by not maintaining Requestor’s proposed rejection of claim 1, based on Farmwald ‘755 and Lu, and also, claims 2-13, 15, 16, 18-22, and 24-35 because the parties and the Examiner focus on the alleged deficiencies of the rejection of claim 1.

2) Farmwald ‘755 and iRAM

Under another rationale involving the proposed rejection based on Farmwald ‘755 and iRAM, Appellant cites iRAM to show “that it would have been obvious to combine the transceiver and DRAMs of Farmwald’s primary bus unit onto a single chip.” (App. Br. 19.) In other words, this rejection proposes integrating Farmwald ‘755’s memory stick components into a single chip. As such, the Examiner’s and Respondent’s teaching away rationale based on defeating chip expansion on the memory stick may be more applicable here - but it is not persuasive. That is, even if a manufacturer would have produced memory sticks for the purpose of

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providing a customer the option of adding more DRAM chips to the memory stick as the Examiner and Respondent maintain, it does not follow that other customers would not have desired a large amount of memory in a single integrated chip, based on the reasons discussed *supra*. For example, such a chip would have offered speed, compactness, efficiency, and durability based on the integration, universal desires carrying implicit motivation according to *Dystar*, 464 F.3d at 1368). As also noted *supra*, Farmwald ‘755 teaches a natural progression by the industry toward such memory expansion on single chips (*e.g.*, for a chip having a constant number of pins). (*See* FW2, FW3.)

Appellant quotes iRAM to show that “[a] sensible alternative is to integrate the memory controller circuits into the memory – completely freeing the CPU of this task. . . . [T]his approach . . . eliminat[es] the design problems associated with refresh and timing. . . . [and also] permits a very simple interface to the CPU and yet provides guaranteed refresh, optimized timing, and minimal hardware support requirements.” (App. Br. 20 (quoting iRAM at 3-433).) Appellant also maintains that the claims involve “nothing more than conventional logic combined with conventional memory.” (App. Br. 21.)

Respondent responds, *inter alia*, that no benefit would redound from such a combination because “the memory controller [in Farmwald ‘755] would behave in the same way and would require the same control signals with the transceiver on the DRAM or off the DRAM.” (Resp. Br. 19.) Appellant’s arguments show that modifying Farmwald’s transceiver so that it is integrated with a DRAM chip would have required minimal changes to the system memory controller. And these arguments do not refute the

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finding of universal benefits of speed, compactness, efficiency, and durability, or the benefit in Farmwald ‘755 of expanding single-chip (internal) memory while maintaining a fixed number of pins on such an integrated device.

Farmwald ‘755 also supports what iRAM teaches: i.e., Farmwald ‘755 teaches a natural growth in the industry toward enhanced memory DRAMs (FW3), and that integrating new circuits and logic into existing single-chip DRAMs was routine (FW 5, FW9, FW10). Moreover, iRAM assumes an *integrated* memory device (i.e., iRAM means integrated RAM) and teaches shifting some of the CPU tasks to this integrated RAM, relieving the CPU of hardware and transceiver functions. (iRAM 1-1; 3-432-433.⁴) In other words, iRAM teaches integrating more functions into a single device, an integrated memory, to relieve the CPU.

Appellant’s arguments that a CPU would act the same regardless of whether functions were transferred from the CPU to a memory chip or memory stick (*see* App. Br. 19) fail to show with persuasive evidence that a non-integrated memory stick device would be as fast (or as compact or durable) as an integrated DRAM. In other words, iRAM points skilled artisans towards an integrated memory – based, for example, on the noted universal desires. Appellant argues that the proposed modification would decrease speed (*id.*, citing Farmwald ‘755 at col. 21, ll. 27-34 and Murphy Supp. Decl. at ¶¶ 48-50), but this contention is not supported, nor does it

⁴ These latter pages, i.e., 3-432, etc., appear under headings of “AP-132” on each page, which appear to signify an attached application note by John J. Fallin and William H. Righter (Intel. Corp. 1982). (*See* iRAM at 3-431.)

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contradict the other universal desires listed in *Dystar* (for compactness, durability, and efficiency). That is, Mr. Murphy relies on the passage at col. 21 in Farmwald ‘755 (Murphy Supp. Decl. at ¶50) to show speed reduction, but Mr. Murphy does not explain why this occurs.⁵ The passage only shows, at most, that a delay of two cycles is required in the transceiver device due to the bus speed, but this does not show that such a delay (even if consequential), is also not required for a DRAM or a group of DRAMs. It also fails to rebut the common sense and supported fact here that an integrated transceiver and DRAM would be faster than a non-integrated transceiver and DRAM merely based on the distance (propagation delay) between the two.

Respondent also does not contend that skilled artisans would have lacked the capability to integrate the memory stick components based on this universal desire for speed or compactness. *See Dystar*, 464 F.3d at 1368. And iRAM’s teaching of “optimized timing” (4-433) also suggests this speed benefit since an integrated memory minimizes component distance and consequent propagation delays as noted *supra*, allowing for optimal timing.

Pursuant to the foregoing discussion, the Examiner erred by not maintaining Requestor’s proposed rejection of claim 1, based on Farmwald ‘755 and Lu, and also, the proposed rejection of claims 2-13, 15, 16, 18-22,

⁵ In reference to the earlier Murphy Declaration, Mr. Parris states as indicated *supra* that Mr. Murphy fails to provide a reason why “moving logic on-chip” would decrease speed, and explains that physically closer devices increase speed. (Parris Decl. ¶ 19.) Mr. Parris’s testimony applies with equal force here.

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and 24-35, because Appellant and the Examiner focus on the alleged deficiencies of the rejection of claim 1. (See App. Br. 19-20; Ans. 18-22.)

Farmwald '755 with Lu and Kushiyama

Obviousness of claims 17, 36, and 37

The Examiner erred by not maintaining Requestor's proposed rejection of claims 17, 36, and 37, based on Farmwald '755, Lu, and Kushiyama, because Appellant and the Examiner focus on the alleged deficiencies of the rejection of claim 1. (See App. Br. 20; Ans. 21.)

Remaining Proposed Rejections

Reversal of the failure to maintain the rejections for all claims on appeal, claims 1-37, makes it unnecessary to reach the remaining rejections for double patenting and anticipation based on Farmwald '037, and for obviousness based, *inter alia*, on Barth. Cf. *In re Gleave*, 560 F.3d 1331, 1338 (Fed. Cir. 2009) (not reaching obviousness after finding anticipation).

DECISION

The Examiner's decision not to reject appealed claims 1-37 is reversed.⁶

REVERSED

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⁶ See Bd.R. 41.77(b) (reversal of determination not to reject is denominated a new ground of rejection).

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